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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of — Confirmation No.: 1735

Stan W. BOWLIN — Art Unit: 2189

S. N. 09/675,974 — Examiner: C. E. Lee

Filed: September 29, 2000

For: METHOD AND APPARATUS FOR RAPID DATA TRANSFER BETWEEN DISSIMILAR DEVICES

NEW BRIEF ON BEHALF OF APPELLANT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an appeal from the Examiner's final rejection mailed August 11, 2003. This new brief is in response to the notification mailed June 14, 2004.

REAL PARTY IN INTEREST

The real party in interest is Fluke Corporation, the assignee of the application.

RELATED APPEALS AND INTERFERENCES

No related appeals or interferences are known to appellant, the appellant's legal representative, or assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF CLAIMS

Claims 1-19 are pending in the application, are rejected, and are the claims under appeal. Appellant wishes to prosecute this appeal with respect to claims 1-19. An appendix of claims is included herewith.

This application was originally filed on September 29, 2000, with claims 1-9. A first office action was mailed February 12, 2003, and a response to that action was filed June 8, 2003, amending claims and adding new claims. A final office action was mailed August 11, 2003, and a response after final was filed November 12, 2003. The Examiner issued an advisory action November 26, 2003, maintaining the rejections, but noting that amendments after final would not be entered for purposes of appeal. Applicant filed a notice of appeal by fax on January 11, 2004, to which this present appeal brief relates.

STATUS OF AMENDMENTS

An amendment was filed subsequent to final rejection, but was not entered. In that amendment, claims 5, 6 and 7 were modified slightly to add redundantly clarifying language to make it redundantly clear that the at least one destination referred to is the at least one of the at least two destinations. It is, however, clear without the amendment what is referred to by the "at least one destinations". Claims 10 and 11 were amended in the after final amendment, to correct a typographical error. The claims stated "said FIFO device" but it is clear from the context

that what was intended and what is meant is "said FIFO data source" since the only FIFO reference in claim 9 (the parent of claims 10 and 11) is a FIFO data source.

Also after final, new claims 20-27 were added to attempt to present the invention in a manner which would be more readily apparent to the Examiner. Since the amendments after final were not entered, the appendix of claims here lists only the claims 1-19 in the form before the amendment after final.

SUMMARY OF THE INVENTION

The invention relates to a manner of speeding data transfer in a device to, in a particular embodiment, enable getting data from a media access controller and to store it both in a memory and to supply the data to a digital signal processing (DSP) chip at the same time, rather than in the traditional fashion of having the DSP chip read the data and then later write the data to memory. To accomplish this, applicant is essentially supplying the data to one device as a read operation, while supplying the data to another device as a write operation, substantially at the same time. Referring to FIG. 1, a DSP microprocessor 20 and SDRAM 18 reside on a BUS 16. In the particular embodiment, data from a network is being supplied to the bus via a MAC 14 (media access controller). The MAC is a FIFO (first-in first-out) device and does not provide an address access to or output for the data it receives. Both the SDRAM and

DSP, on the other hand, use addressing schemes for access storage of data. Rather than adhere to the prior art mode of having the DSP read the data from the bus as supplied to the bus by the MAC, and then, later writing the data to the SDRAM, applicant's invention as data is retrieved onto the bus from the MAC, it is substantially simultaneously written to a storage address in the SDRAM and is read by the DSP. Should the DSP later decide that the data is to be discarded, the address pointers for the SDRAM are not advanced and the next data will write over the discarded data. This saves time for operations where the computing power of the DSP is to be used to the maximum possible extent. (Specification, page 3, line 5-24). FIG. 2 shows a timing chart of a particular embodiment in operation. Timing is controlled by CPLD 22 (FIG. 1). Signals 24, 26 and 28 are from the DSP and represent clock (24), a command signal (26) and an address signal (28) which is used to select row and column in the SDRAM (page 3, lines 25-35).

Signals 30 and 32 are SDRAM signals (command, 30 and row/column address 32).

Signal 34 is the received data from the MAC. (page 4 lines 1-8)

Thus in operation, the various timing of set up and running is discussed at page 4, line 10 - page 5 line 7.

The various operations from time 1 to 6/7 are done to set the operation up and at time T6/7-T13, the MAC data on signal 34 is thereby substantially simultaneously supplied to the SDRAM and to the DSP.

The DSP is operating as if performing read cycles, while the SDRAM is operating as if performing write cycles.

THE ISSUES

The broad issue presented in this appeal is whether the Examiner's final rejection of claims 1-19 is proper. The issue may be stated more narrowly as:

1. Whether claims 1-19 are unpatentable under 35 U.S.C. 112, first paragraph, because the specification is not enabling for transferring a unit of data on a bus from a source to at least two destinations substantially simultaneously.

2. Whether claims 10 and 11 are indefinite under 35 U.S.C. 112, second paragraph.

3. Whether claims 1, 4-8, 12, 14-16 and 19 are unpatentable under 35 U.S.C. 103(a) over Applicant Admitted Prior Art in view of Masterson et al (U.S. 5,073,851).

4. Whether claims 2, 3, 9-11 and 13 are unpatentable under 35 U.S.C. 103(a) over Applicant Admitted Prior Art in view of Masterson et al (U.S. 5,073,851) and further in view of DeSouza et al (U.S. 5,379,289).

5. Whether claims 17 and 18 are unpatentable under 35 U.S.C. 103(a) over Applicant Admitted Prior Art in view of Masterson et al (U.S. 5,073,851) and further in view of IBM_TDB December 1979, Vol. 22, Issue No. 7, pages 2651-2654.

GROUPING OF CLAIMS

Claims 1-9 and 12-19 stand or fall together but do not necessarily stand or fall with claims 10 and 11. Claims 10 and 11 stand or fall together but do not necessarily stand or fall with claims 1-9 and 12-19. If the amendment after final to claims 10 and 11 is entered, then claims 1-19 stand or fall together. However, if the amendment after final is not entered, the claims stand or fall separately because resolution of the section 112, second paragraph rejection against applicant for claims 10 and 11 would not affect claims 1-9 and 12-19, since those claims do not have the complained of language that they Examiner relies on to reject claims 10 and 11.

ARGUMENT

1. Claims 1-19 are patentable and are enabled under 35 U.S.C. 112, first paragraph. The Examiner rejected claims 1-19, stating that the specification is not enabling for transferring a unit of data on a bust from a source to at least two destinations substantially simultaneously. Applicant respectfully disagrees.

It is believed by applicant that the Examiner is misinterpreting or misunderstanding what is shown in the specification and drawings.

The Examiner says that applicant admits in the specification that there is a 2 cycle delay in a read operation and that therefore the transfer to at least two destinations substantially simultaneously is not enabled. Applicant disagrees. The timing chart and portion of the specification in question merely shows the timing of signals to set the DSP chip into a read operation. The RX_Data 34 appears on the bus for reading by the DSP and writing to the memory storage only at the timing shown. That is, at cycle 9, for example, data W3 is present on the bus. That is the only time that the transfer from the bus to both the DSP and the memory device can be effected for a specific data unit (W3, in the example discussed herein). The data cannot start being read by the DSP from the bus before it appears on the bus. Similarly, the data cannot be read after it is no longer on the bus. Applicant respectfully submits that the specification is enabling for what is claimed. The data is present for a set period of time (typically one clock cycle, but in the case of W1, it is 2 clock cycles in the particular embodiment illustrated) and during that time transfer to the first data source as a read and to the second data source as a write are effected. Merely because the timing of operation

of one device in the illustrated example requires a read signal to be enabled before the read data is present does not make the specification non-enabling. It only shows the timing required for supplying signals to the various devices to get them to behave in the manner applicant desires in this embodiment. Further, the specification at page 4, lines 23-24, referred to by the Examiner, is merely stating that in the particular timing required, first, row address data is supplied to the memory device, then, 2 clock cycles later, a READ signal is supplied on the DSP device command signal line and the column selection signal COL is supplied to the memory device. This does not state that a 2 cycle latency is present between a read and a write. It merely teaches the timing of the control signals to effect the various devices to properly access the data in the RX_Data bus during the short time that each data W1, W2, W3, etc., is present.

Paraphrasing what the Examiner says, he seems to be looking at the timing chart of FIG. 2 and say that the write command at time T7 is the "write operation" and so that the data on the received data line at time T9 has already been written at time T7.

This interpretation is not correct and would not be possible in a world such as ours where time is linear. The data at time T9 in the timing chart could not be written at time T7,

because the data of time T9 has not appeared until time T9. At time T7, data word #1 is being written. The data at time T9 is data word #3.

Applicant believes the Examiner is mis-interpreting the WRITE control signal to the memory chip. That signal just starts the writing, and writing then continues each clock cycle until the stop command appears later on at time T14 in FIG. 2.

It is respectfully submitted that the specification is enabling. The Examiner states that he "doubts how to transfer a unit of data on a bus from a source to at least two destinations substantially simultaneously", but as noted above, the Examiner's discussion of what he believes to be happening is unusual in that it talks about accessing data at a time T7 on the timing chart where the data is not available until time T9.

The Examiner says that applicant admits that there are 2 clock cycles latency between a read data operation and a write data operation (referring to page 4, lines 23-24). This is not at all what applicant is stating. Applicant is merely discussing in that portion of the specification the specific timing of a disclosed embodiment of the invention is setting up the various chips in order to have the invention be accomplished, and in that case, setting up the memory chip involves setting row data at a certain time and then, two clock cycles later, the column data is set. It is not "admitting that

there are two clock cycles latency between a read data operation and a write data operation.

2. Claims 10 and 11 are definite. While it is clear that claims 10 and 11 had typographical errors in them, applicant had attempted to correct the errors in the amendment after final, but it was not entered. It is readily apparent what applicant meant, and the Examiner even notes what applicant meant, but rather than allow entry of the correction of a typographical error, the 35 U.S.C. 112 second paragraph rejection was maintained. Applicant respectfully asks that the typographical error be corrected since it is clear what is meant by applicant. Even without correction, it is clear what the claims mean.

3, 4 and 5. Claims 1-19 are patentable over Applicant Admitted Prior Art in view of Masterson et al (U.S. 5,073,851) (claims 1, 4-8, 12, 14-16 and 19), and further in view of DeSouza (claims 2, 3, 9-11 and 13) and further in view of IBM_TDB December 1979, Vol. 22, Issue No. 7, pages 2651-2654 (claims 17 and 18).

The applicant's admitted prior art (AAPA) as discussed in the application involved reading data, and then, after deciding whether to save the data, writing the data if it is decided to save it.

Thus, the applicant's admitted prior art, as cited by the Examiner, performs operations like this:

At time T1, read word #1 into device1, no write

at time T2, read word #2 into device1, write word #1 to device2

at time T3, read word #3 into device1, write word #2 to device2, etc.

The Examiner then combines the prior art discussed in the application with the cited art (Masterson and others) to say the invention is thereby obvious. Applicant respectfully submits that it would not be obvious.

Applicant's invention would be this form of operation:

At time T1, read word #1 into device1, write word #1 into device2

At time T2, read word #2 into device1, write word #2 into device2

At time T3, read word #3 into device1, write word #3 into device2, etc.

Thus, the prior art is not at all doing what applicant is doing. The prior art is not transferring a unit of data to at least two destinations substantially simultaneously by supplying the data from the source to a first destination as a read operation and to a second destination as a write operation. In the prior art, at time T1, there is only a read, no write. But then, at time T2, there are both read and writes, but the read and writes do not involve a unit of data - they involve separate

data items. The prior art does not even appreciate the concept of what applicant is doing, as the prior art is concerned with some other issues or problems entirely.

A reason for applicant doing all this operation was need for speed. The inventor discovered that by doing this, operation of his device could be speeded up by not having to read, decide whether they wanted to keep the data in memory, and then write (or not write if they didn't want to keep the data).

By doing it this way, the data is always simultaneously written to memory while it is being read into the DSP chip, and if it is not desired to keep the data in memory for whatever reason (say, for example, the data has errors and is to be discarded), then one simply does not advance the memory storage location pointer so that the next new data coming in later overwrites the portion in memory where the data was written but is to be discarded.

This speeds things up to take advantage of the available computing power and get done more operations in a given time constraint.

The prior art isn't concerned with this.

Masterson is concerned with transferring data between memory and cache. If memory were considered DEV#1 (abbreviation for device #1) and cache were considered DEV#2 (abbreviation for

device #2), then the operation taught by Masterson is as follows for transfer of N data units:

At Time T1, Read 1st data from DEV#1, no operation in DEV#2

At T2, Read 2nd data from DEV#1, write 1st data to DEV#2

At T3, Read 3rd data from DEV#1, write 2nd data to DEV#2

. . .

At Time N, Read Nth data from DEV#1, write N-1st data to DEV#2

At Time N+1, no read operation, write Nth data to DEV#2.

This is not related to what applicant claims.

Discussing the operation of applicant's methods and devices in a similar format to the above discussion of Masterson's operation, applicant's operations would be as follows:

Assuming DEVA is device A, a first device, and DEVB is device B, a second device, to transfer N data units:

At Time T1, DEVA reads first data, DEVB writes first data

At Time T2, DEVA reads second data, DEVB writes second data

At Time T3, DEVA reads third data, DEVB writes third data

. . .

At Time N, DEVA reads Nth data, DEVB writes Nth data.

The above illustrates a difference. Masterson specifically teaches away from applicant's claimed invention. Even if Masterson were related to applicant's invention (which it is not), to transfer N units of data requires N+1 operation cycles

in Masterson. It requires N operation cycles in applicant's manner of operation.

Claim 1 discusses, removing some of the details in order to illustrate applicant's point, transferring **a unit** of data, which includes supplying **said unit** of data to a first destination and supplying **said unit** of data to a second destination. In making the rejection, the Examiner has instead converted this to be transferring a **first data** to device #1 and transferring a **second data** to device #2. But that is not what applicant claims.

The Examiner indicates that it is assumed that the "a unit of data" for a read operation is different from the subject matter "unit of data" for a write operation. So, what the Examiner is rejecting is not even what is recited in the claims. Instead, the Examiner is changing the interpretation of what the claims say into something different than what they say. Note the emphasized portions above. A purpose of applicant's invention is to speed operations, to avoid having to transfer data across a bus twice. Thus an advantage is provided as a unit of data is substantially simultaneously written to one device while another device is reading the unit of data. That is the same unit of data. The timing chart of FIG 2 shows item 34, that the data appears on the bus once. It is not repeated. This speeds operation.

A corresponding argument applies to claim 8, wherein the selected ones of discrete units of data are written to the memory and read to the microprocessor substantially simultaneously. Claim 8 is also therefore allowable.

The respective dependent claims are also submitted to be allowable.

Claims 2, 3, 9-11 and 13 rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over AAPA in view of Masterson and further in view of DeSouza et al, U.S. 5,379,289. Applicant respectfully traverses.

DeSouza adds nothing that would overcome the conceptual difference between Masterson and applicant's methods and devices as noted above. Even if there were motivation to combine these documents' teachings, the resulting device and methods would still carry the above-noted difference wherein while first data is read, no data is written, and when second data is read, the first data is written, etc., requiring N+1 steps for N data. This explicitly teaches away from applicant's simultaneous read/write concept. Therefore, claims 2, 3, 9-11 and 13 are submitted to be allowable.

Claims 17 and 18 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over AAPA in view of Masterson and further in view of IBM Technical Disclosure Bulletin, December

1979, Circuit for Tracing Branch Instructions. Applicant respectfully traverses.

The IBM bulletin relates to a system for providing an audit trail of branch instructions. So, an instruction address register is recorded, but an address pointer is not incremented until a branch instruction occurs. Thus, only the points where branch instruction addresses occur are recorded. The purpose is to not fill the trace memory to its capacity, by only recording branch instruction addresses, rather than all addresses. It is respectfully submitted that one would not look to circuits for avoiding filling trace memory when tracing branch instructions in a processor under test when constructing methods and devices such as applicant's, wherein the goal is to speed operations rather than to save memory capacity.

However, even if one were motivated to look to the IBM bulletin, the lack of teaching by Masterson as discussed above is not changed by the addition of the IBM bulletin. Accordingly claims 17 and 18 are submitted to be allowable.

In view of these points above, it is respectfully submitted that the rejection under 35 U.S.C. §103(a) should not be sustained.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-19 of this application are patentable, and it is accordingly requested that the Examiner's final rejection be reversed and that allowance of this application be directed. The newly presented claims after final, 20-27, which were not entered by the Examiner, but for which applicant would respectfully request entry now, would also be allowable for corresponding reasons. These new claims were attempted to be added to provide a slightly altered manner of claiming the invention, in hope that the variation therein would assist the Examiner to understand the inventive concepts.

Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Confirmation No.: 1735

Stan W. BOWLIN Art Unit: 2189

S. N. 09/675,974 Examiner: C. E. Lee

Filed: September 29, 2000

For: METHOD AND APPARATUS FOR RAPID DATA TRANSFER BETWEEN DISSIMILAR DEVICES

APPENDIX OF CLAIMS WITH AMENDMENT AFTER FINAL NOT ENTERED

1. (previously amended) A method for transferring a unit of data on a bus from a source to at least two destinations substantially simultaneously, comprising the steps of:

supplying said unit of data from the source to first of said at least two destinations as a read data operation; and

supplying said unit of data to a second of said at least two destinations as a write operation.

2. (original) The method according to claim 1, wherein the source comprises a non-addressed data device.

3. (original) The method according to claim 2, wherein the source comprises a FIFO device.

4. (original) The method according to claim 1, wherein at least one of the at least two destinations comprise addressed data devices.

5. (original) The method according to claim 4, wherein the at least one destinations comprises a microprocessor.

6. (original) The method according to claim 4, wherein the at least one destinations comprises a memory storage.

7. (original) The method according to claim 4, wherein the at least one destinations comprises a SDRAM memory.

8. (previously amended) An apparatus for transferring received data in discrete units from a network, comprising:

a bus;

a media access controller for putting ones of discrete units of the received data from the network onto said bus;

a microprocessor for reading the ones of discrete units of data from said bus;

a memory for writing the ones of discrete units of data from said bus into said memory; and

a timing controller for controlling said media access controller, said microprocessor and said memory to have said media access controller write selected ones of discrete units of the data to the bus, said memory write said selected ones of discrete units of the data to said memory and said microprocessor read said selected ones of discrete units of the data substantially simultaneously.

9. (previously amended) An apparatus for transferring data, comprising:

a bus;

a FIFO data source connected to said bus for putting data onto said bus;

a microprocessor connected to said bus for reading the data from said bus;

a memory connected to said bus for writing the data from said bus into said memory; and

a timing controller connected to said FIFO data source, said microprocessor and said memory for controlling said FIFO data source, said microprocessor and said memory to have said FIFO data source put the data onto the bus, and for a selected quantity of data, have said memory write the selected quantity of data to said memory and said microprocessor read the selected quantity of data substantially simultaneously.

10. (previously presented) The apparatus for transferring data according to claim 9, wherein said FIFO device is a media access controller.

11. (previously presented) The apparatus for transferring data according to claim 9, wherein said apparatus is a network test instrument and said FIFO device is a media access controller.

12. (previously presented) The method according to claim 1, wherein said supplying as a read and write operation of said unit of data is accomplished with said unit of data being presented on said bus as a single instance.

13. (previously presented) The method according to claim 2, wherein the source comprises a media access controller device.

14. (previously presented) An apparatus for transferring received data in discrete units from a network according to claim 8, wherein said apparatus comprises a network test instrument.

15. (previously presented) An apparatus for transferring received data in discrete units from a network according to claim 8, wherein said memory write of the selected quantity of data to said memory and said microprocessor read of the selected quantity of data are accomplished with said selected quantity of data being presented on said bus as a single instance.

16. (previously presented) A method for operating a network test instrument to transfer data on a bus within said network test instrument from a media access controller at least to a processor and to a memory, separate from said processor, comprising the steps of:

supplying said data from the media access controller to said processor as a read data operation performed by said processor; and

supplying said data to said memory as a write operation,

wherein said step of supplying data to said processor and said step of supplying data to said memory are accomplished substantially simultaneously with use of the same transfer of said data on said bus.

17. (previously presented) The method for operating a network test instrument according to claim 16, further comprising the steps of:

determining whether the data currently transferred to said memory is to be retained before a next data is transferred said memory, and if said data currently transferred is to be retained, modifying a next data write address location so that a next data does not overwrite the data currently transferred, and otherwise, if said data currently transferred is not to be retained in said memory, keeping the next data write address as a current data write address value so that the next data is written over the data currently transferred.

18. (previously presented) The method for transferring according to claim 7, further comprising the steps of:

determining whether the unit of data currently transferred to said SDRAM is to be retained before a next unit of data is transferred said SDRAM, and if said unit of data currently transferred is to be retained, modifying a next data write address location so that a next unit of data does not overwrite

the unit of data currently transferred, and otherwise, if said unit of data currently transferred is not to be retained in said SDRAM, keeping the next data write address as a current data write address value so that the next unit of data is written over the unit of data currently transferred.

19. (previously presented) The method for transferring according to claim 1, wherein said unit of data comprises a word.